What is claimed is:

- 1. A circuit for delaying power interruption to a non-volatile memory device comprising: a power supply having an output connected to the non-volatile memory device; a charge-storing device connected to the output of the power supply; and,
- a DC-to-DC converter connected at its input to the charge-storing device and the power supply and connected at its output to the non-volatile memory device such that upon interruption of the power supply, the charge-storing device provides sufficient input voltage to the DC-to-DC converter to provide rated output to the non-volatile memory device for a time sufficient for the non-volatile memory device to complete a write cycle.
- 2. A voltage booster circuit as recited in claim 1 wherein the charge-storing device is a capacitor.
- 3. A voltage booster circuit as recited in claim 1 wherein the charge-storing device is an electrolytic capacitor.
- 4. A voltage booster circuit as recited in claim 1 wherein the charge-storing device is a super capacitor.
- 5. A voltage booster circuit as recited in claim 1 wherein the charge-storing device comprises a plurality of capacitors connected in parallel.
- 6. A voltage booster circuit as recited in claim 1 further comprising an inductor connected in parallel with the DC-to-DC converter.
- 7. A voltage booster circuit as recited in claim 6 further comprising a diode connected in series between the inductor and the output of the DC-to-DC converter.

- 8. A voltage booster circuit as recited in claim 1 further comprising a diode at the input of the charge storing device connected such that the flow of electric current from the charge-storing device to the power supply is prevented.
- 9. A method of supplying power to a non-volatile memory device comprising: providing a charge-storing device; connecting the input of a DC-to-DC converter to the charge-storing device; and, connecting the output of the DC-to-DC converter to the non-volatile memory device.
- 10. A method of supplying power to a non-volatile memory device comprising: providing regulated power from a power supply; storing electrical charge from the power supply in a charge-storing device; transferring the stored electrical charge upon interruption of the power supply to the input of a DC-to-DC converter at a potential sufficient to operate the DC-to-DC converter; and
- supplying regulated DC power from the output of the DC-to-DC converter to the non-volatile memory device for a time sufficient for the non-volatile memory device to complete a full write cycle.
- 11. A method of preventing data corruption in a non-volatile memory device comprising: determining whether a control signal sent to the non-volatile memory device is a reset signal; delaying the control signal if the control signal is a reset signal for time sufficient for the non-volatile memory device to complete a memory write cycle.
- 12. A method of preventing data corruption in a non-volatile memory device in a processor-based system comprising: intercepting control signals sent to the non-volatile memory device; determining whether a control signal sent to the non-volatile memory device is a reset signal; delaying the control signal if the control signal is a reset signal for time sufficient for the non-volatile memory device to complete a memory write cycle.

- 13. A method as recited in claim 12 wherein the reset signal is sent by the processor.
- 14. A method as recited in claim 12 wherein the reset signal is sent by a power monitor.
- 15. A method of preventing data corruption in a non-volatile memory device comprising: determining whether a control signal sent to the non-volatile memory device is a reset signal; starting a timer if the control signal is a reset signal; sending the reset control signal to the non-volatile memory device after a pre-selected time interval.
- 16. A method as recited in claim 15 wherein the pre-selected time interval is equal to or greater than the time required for the non-volatile memory device to complete a memory write cycle.
- 17. A method of preventing data corruption in a non-volatile memory device comprising: determining whether a control signal sent to the non-volatile memory device is a reset signal; delaying the control signal if the control signal is a reset signal for time sufficient for the non-volatile memory device to complete a memory write cycle; providing regulated power from a power supply to the non-volatile memory device; storing electrical charge from the power supply in a charge-storing device; transferring the stored electrical charge upon interruption of the power supply to the input of a DC-to-DC converter at a potential sufficient to operate the DC-to-DC converter; and
- supplying regulated DC power from the output of the DC-to-DC converter to the non-volatile memory device for a time sufficient for the non-volatile memory device to complete a write cycle.
- 18. A method as recited in claim 17 wherein the non-volatile memory device is a flash memory.

- 19. A method as recited in claim 18 wherein the flash memory is a NAND-type flash memory.
- 20. A circuit as recited in claim 1 wherein the non-volatile memory device is a NAND-type flash memory.